Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of forming silicides on first and second transistors, where the transistors are formed upon a silicon substrate and include respective silicon gate stacks, and where the silicon gate stacks and exposed portions of the substrate are covered in a layer of oxide material and where portions of the layer of oxide material are covered by respective sidewall spacers formed adjacent the gate stacks, the method comprising:

forming a layer of masking material over the second transistor;

removing ~~the~~ exposed portions of the layer of oxide material from the first transistor, thereby exposing a top portion of the silicon gate stack of the first transistor;

removing the masking material from the second transistor;

forming a first layer of metal material over both of the transistors;

forming a first silicide on the exposed top portion of the silicon gate stack of the first transistor;

removing unreacted first layer of metal material thus exposing oxide material;

removing ~~the~~ exposed oxide material from the second transistor, thereby exposing a top portion of the silicon gate stack of the second transistor;

forming a second layer of metal material over both of the transistors;

forming a second silicide on the exposed top portion of the silicon gate stack of the second transistor; and

forming a secondary silicide on the first silicide formed on the top portion of the silicon gate stack of the first transistor.

2. (Original) The method of claim 1, wherein removing exposed oxide material from the first transistor exposes portions of the silicon substrate above source and drain regions formed within the substrate adjacent the gate stack of the first

transistor, and wherein removing exposed oxide material from the second transistor exposes portions of the silicon substrate above source and drain regions formed within the substrate adjacent the gate stack of the second transistor, the method further comprising:

forming additional first silicides on the exposed portions of the substrate adjacent the gate stack of the first transistor when the first silicide is formed; and

forming additional second silicides on the exposed portions of the substrate adjacent the gate stack of the second transistor when the second silicide is formed.

3. (Original) The method of claim 1, further comprising:
removing un-reacted metal material after forming the first silicide; and
removing un-reacted metal material after forming the second silicide.

4. (Original) The method of claim 1, wherein the exposed oxide material is removed from the first transistor via etching.

5. (Original) The method of claim 1, wherein the exposed oxide material is removed from the second transistor via etching.

6. (Original) The method of claim 1, wherein the first, second and secondary silicides are formed via a heat treatment.

7. (Original) The method of claim 1, wherein the first metal material comprises cobalt and/or a cobalt containing compound.

8. (Original) The method of claim 1, wherein the second metal material comprises nickel and/or a nickel containing compound.

9. (Original) The method of claim 1, wherein the first silicide is formed via heating to around 800 to 900 degrees Celsius.

10. (Original) The method of claim 1, wherein the second silicide is formed via heating to around 500 to 600 degrees Celsius.

11. (Original) The method of claim 1, wherein the first metal material comprises cobalt and/or a cobalt containing compound and the first silicide is formed via heating to around 800 to 900 degrees Celsius.

12. (Original) The method of claim 1, wherein the second metal material comprises nickel and/or a nickel containing compound and the second silicide is formed via heating to around 500 to 600 degrees Celsius.

13. (Original) The method of claim 1, wherein the first transistor is an NMOS transistor and the second transistor is a PMOS transistor.

14. (Original) The method of claim 13, wherein areas of the substrate underlying the first transistor serve as a P-well and areas of the substrate underlying the second transistor serve as an N-well.

15. (Original) The method of claim 14, wherein areas of the substrate adjacent the gate stack of the first transistor are doped to produce first source and drain regions, and areas of the substrate adjacent the gate stack of the second transistor are doped to produce second source and drain regions.

16. (Original) The method of claim 15, wherein the first source and drain regions are doped with phosphorous or other N-type dopants and the second source and drain regions are doped with boron or other P-type dopants.

17. (Original) The method of claim 3, wherein un-reacted metal material is removed after the first and second silicides are formed via a wet strip.

18-20 (Cancelled).